

**architecture exploration of fpga based accelerators for ...** - architecture exploration of fpga based accelerators for bioinformatics applications by b. sharat chandra varma amar nath and shashi khosla school of information technology **visualization support for fpga architecture exploration** - visualization support for fpga architecture exploration by k. nasartschuk, k. b. kent and r. herpers tr 11-213, december 1, 2011 faculty of computer science **architecture exploration for hls-oriented fpga debug overlays** - what this talk is about! recent work: source-level, in-system debugging of hls circuits! debug instrumentation is inserted at compile time! changing this instrumentation (to trace **efficient bindct hardware architecture exploration and ...** - original article e! efficient bindct hardware architecture exploration and implementation on fpga abdessalem ben abdelalia,b,\*, ichraf chattia, marwa hannachia,c, **automated transistor sizing for fpga architecture exploration** - automated transistor sizing for fpga architecture exploration ian kuon and jonathan rose the edward s. rogers sr. department of electrical and computer engineering, **design space exploration for image processing ...** - design space exploration for image processing architectures on fpga targets chandrajit pal, avik kotal, asit samanta, amlan chakrabarti, ranjan ghosh **the vtr project: architecture and cad for fpgas from ...** - the exploration of new programmable architectures, and the development of innovative algorithms required to synthesize circuits into fpgas requires a robust software tool that permits experimentation. in order to model modern and future architectures, such a tool is necessarily quite complex, and largely beyond the capacity of any single academic enterprise to create, evolve and maintain ... **fpreso: enabling express transistor-level exploration of ...** - full and thus unusable to drive realistic fpga architecture exploration. the other possibility is the one attempted by chiasson and betz with coffe [4]: reduce the complexity of transistor size optimization in an fpga by exploiting the structure of the circuit and by building a tool implementing ad hoc but efficient optimization strategies. the result is a reference and parameterizable ... **exploring networks-on-chip for fpgas** - exploring networks-on-chip for fpgas rosemary m. francis summary developments in fabrication processes have shifted the cost ratio between wires and transistors **efficient heterogeneous architecture floorplan optimization ...** - in this paper we define the fpga architecture exploration problem as finding an optimal layout of the fpga chip, and positioning circuit blocks while minimizing an objective function comprising selected performance metrics. **chapter 6 three-dimensional tree-based fpga: architecture ...** - 118 6 three-dimensional tree-based fpga: architecture exploration tools! of cad tools such as 3d placement and routing. in order to validate the architecture **ieee transactions on computer-aided design of integrated ...** - exploring fpga routing architecture stochastically mingjie lin, member, ieee, john wawrzynek, and abbas el gamal, fellow, ieee abstract! this paper proposes a systematic strategy to efficiently explore the design space of field-programmable gate array (fpga) routing architectures. the key idea is to use stochastic methods to quickly locate near-optimal solutions in designing fpga routing ... **exploration of pipelined fpga interconnect structures** - rapid [4] architecture identify tradeoffs that must be made while designing the interconnect structure of a pipelined fpga. the post-exploration architecture that we found shows a 19%

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